1. (Amended) A ferroelectric memory cell for use in a ferroelectric random access memory (FeRAM) device, the ferroelectric memory cell comprising:

a first active area incorporating therein a gate of a depletion mode transistor;

a second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor;

a word line coupled to the gate of the depletion mode transistor and the gate of the enhancement mode transistor; and

a ferroelectric capacitor having first and second terminals, the first terminal coupled to a drain of the enhancement mode transistor and the second terminal coupled to a cell plate, for storing data.

5. (Amended) A ferroelectric random access memory (FeRAM) device including a plurality of ferroelectric memory cells, comprising:

first active areas incorporating therein gates of depletion mode transistors;

second active areas adjacent to the first active areas incorporating therein gates of enhancement mode transistors;

word lines coupled to the gates of the depletion mode transistors and the gates of the enhancement mode transistors; and